1   ABSTRACT

2   An in-order issue in-order completion micro-controller

3   comprises a pipeline core comprising in succession a fetch

4   address stage, a program access stage, a decode stage, a

5   first execution stage, a second execution stage, a memory

6   access stage, and a write back stage. The various stages

7   are provided a thread ID such that alternating stages use a

8   first thread ID, and the other stages use a second thread

9   ID. Each stage which requires access to thread ID specific

10   context information uses the thread ID to specify this

11   context information.